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(((DECOD$3 AND (PARALLEL$7 OR CONCURRENT$4 OR SIMULTANEOUS$3)) AND (EXECUT$5 OR PROCESS$4) NEAR15 (SPECIAL$5 OR ALL OR GENERAL$4) NEAR15 (INSTRUCTION$1 OR COMMAND$1 OR MICRO NEAR1 INSTRUCTION$1 OR COD$3 OR OPCOD$3) AND (FAST$3 OR SLOW$2 OR HIGH$4 OR LOW$3 OR DIFFERENT) NEAR5 (SPEED$1 OR RATE$1) NEAR45 (DATABUS$3 OR BUS$3 OR CHANNEL$1 OR PATH$1 OR DATAPATH$1 OR CONNECTION$1 OR LINK$3)).CLM.).PGPB.	0

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L29	((decod$3 and (parallel$7 or concurrent$4 or simultaneous$3)) and (execut$5 or process$4) near15 (special$5 or all or general$4) near15 (instruction$1 or command$1 or micro near1 instruction$1 or cod$3 or opcod$3) and (fast$3 or slow$2 or high$4 or low$3 or different) near5 (speed$1 or rate$1) near45 (databus$3 or bus$3 or channel$1 or path$1 or datapath$1 or connection$1 or link$3)).clm.	0	L29
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L27	((execut$5 or process$4) near7 (special$5 or all or general$4) near8 (instruction$1 or command$1 or micro near1 instruction$1 or cod$3 or opcod$3) and (fast$3 or slow$2 or high$4 or low$3 or different) near5 (speed$1 or rate$1) near45 (databus$3 or bus$3 or channel$1 or path$1 or datapath$1 or connection$1 or link$3)).clm.	5	L27
	DB=PGPB,USPT; PLUR=YES; OP=OR		
L26	l5 and l12	8	L26
L25	l5 and l11	7	L25
L24	l5 and l10	0	L24
L23	l5 and l9	1	L23
L22	l5 and l8	18	L22
L21	l5 and l7	228	L21
L20	l5 and l6	308	L20
L19	l3 and l12	9	L19
L18	l3 and l11	12	L18
L17	l3 and l10	1	L17
L16	l3 and l9	2	L16
L15	l3 and l8	22	L15
L14	l3 and l7	290	L14
L13	l3 and l6	380	L13
L12	(713/322,323)[CCLS]	1479	L12
L11	(709/232, 233)![CCLS]	1448	L11
L10	(370/230)![CCLS]	1501	L10
L9	(710/60)![CCLS]	350	L9
L8	(712/245-248)[CCLS]	799	L8

L7	(712/12-226)[CCLS]	9166	L7
L6	(712/2-300)[CCLS]	12602	L6
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L4 and l3	1960	L5
L4	(activat$4 or deactivat$4 or disabl$7 or enabl$7 or "off" or stall$5 or inhibit$3 or halt$3) near5 (execut$3 or process$3)	529917	L4
L3	l1 and L2	3521	L3
L2	(fast$3 or slow$2 or high$4 or low$3 or different) near5 (speed$1 or rate$1) near45 (databus$3 or bus$3 or channel$1 or path$1 or datapath$1 or connection$1 or link$3)	188620	L2
L1	(execut$5 or process$4) near7 (special$5 or all or general$4) near8 (instruction$1 or command$1 or micro near1 instruction$1 or cod$3 or opcod$3)	35502	L1

END OF SEARCH HISTORY

Programmable and automatically-adjustable sense-amplifier activation sche reset address-driven decoding scheme for high-speed reusable SRAM core

Suzuki, T. Nakahara, S. Iwahashi, S. Higeta, K. Kanetani, K. Nambu, H. Yoshida, M. Yamaguchi, K.
Device Dev. Center, Hitachi Ltd., Tokyo, Japan

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Abstract
Describes novel schemes developed to meet the demand for a reusable embedded SRAM core for application to a vari PAS optimizes sense-amplifier **activation** timing by using the combination of a program and automatic control. MRAD r overhead by reducing the fluctuation of **path**-to-**path** delay. These schemes experimentally demonstrated a wide-opera 1.4 V and an access time of 600 ps.

Index Terms
Inspec

Controlled Indexing
SRAM chips application specific integrated circuits **decoding** delays **high-speed** integrated circuits int circuit design memory architecture reconfigurable architectures timing

Non-controlled Indexing
0.5 to 1.4 V 600 ps MRAD PAS SOC design access time automatically-adjustable sense-amplifier ac scheme **high-speed** reusable SRAM core multi-reset address-driven **decoding** scheme **path**-to-**path** de amplifier **activation** timing timing-overhead wide-operation range

Author Keywords
Not Available

References

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Suzuki, T.; Nakahara, S.; Iwahashi, S.; Higeta, K.; Kanetani, K.; Nambu, H.; Yoshida, M.; Yamaguc
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13-15 June 2002 Page(s):44 - 45
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